

- **Advanced Digital design**
 - Combinational & Sequential Ckts
 - Finite State Machines
 - Timing Analysis
 - Complex Circuit Design& Analysis
 - Programmable Devices
- **Introduction to Linux**
 - Linux Architecture
 - Commands& Utilities
 - Scripting(Shell& PERL)
- **Verilog HDL**
 - Introduction & Applications
 - Data types& Operators
 - Assignments
 - Tasks & Functions
 - System Tasks
 - Finite State Machine Coding
 - H/W Inferences of Verilog constructs
- **System Verilog**
 - Basic Constructs
 - Interface
 - OOPS
 - Randomization
 - Functional Coverage
 - Coverage Driven verification
 - SV Assertions
- **Verification Methodology: OVM/UVM**
- **Special Guest lectures**
- **Project from Industry choice**



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 - Data types& Operators
 - Tasks, System tasks & Functions
 - Finite State Machine Coding
 - H/W Inferences of Verilog construct
- **Hardware Design**
 - Schematic Capture
 - PCB layout, SI, Thermal analysis
 - PCB Assembly & Testing Flow
- **Software Design**
 - Overview C
 - Basics of device drivers
 - Drivers for Display, UART etc
 - Introduction to Linux device Driver
- **ARM Controller**
 - Introduction to ARM Cortex M3
 - Architecture & Hands on experiment
- **Special Guest Lectures**
- **Live projects**



M/s Reliable Technosystems (I) Pvt Ltd (RTS), Hyderabad is a 4+ year old, System Solutions & Technology Engineering services organization focussed on Embedded & VLSI Space. RTS is engaged in design, development of DSP / FPGA / Microcontroller/SOC based servo controllers,& High Speed data acquisition systems for DRDO labs over the years. RTS is closely associated with Industry experts for consulting services & corporate trainings. More specifics about the organization can be viewed at:www.reliabletechsys.com

RTS is planning a special training batch for selective aspiring professionals in Embedded & VLSI streams. This is a 3 month, job-focused & placement-guidance-assured training. The course content is unique & covers practical aspects with labs at all appropriate points. Six months stipend paid on job exposure follows 3 months formal training. A pre-test is planned during Mid April 2015 for the batch selections. The proposed team size is 10-12 in each stream. A brief about the course content is attached for an easy reference. The faculty are derived from industry Experts & Veterans.

- *Mr. Anand Moghe (Retired, Ex XILINX, CYPRESS, Mentor Graphics, eInfoChips, CMC)*
- *Mr. Shrawan Vaidya (15+ Ex. Intel)*
- *Mr. MukeshChawhan (15+ Ex. XILINX, Synopsys, Mentor Graphics)*
- *Mr.VamsiRajulapudi (15+ Ex.Moschip, GE, SM Silicon)*

Please contact hr@reliabletechsys.com for further details on **enrolment & course fee**. **Mobile:** 91-9545299993/9701156155(Alit/Narasimha) or Land Line: 040-6514 1288

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ADVANCED VLSI & EMBEDED SYSTEMS TRAINING

